CLAIMS

1. A method for fabricating a transistor with a metal gate, that includes a siliciding phase comprising:

the formation, from a first metal, of a first metal silicide on the drain and source regions, while the gate region is protected by a layer of hard mask;

the removal of the hard mask;

the formation, from a second metal, of a second metal silicide in the entire gate region so as to completely siliciding the gate region, while the first metal silicide is protected by the second metal; and

the removal of the second metal.

2. The method according to Claim 1, wherein the siliciding phase includes a final step of annealing the first metal silicide and of the second metal silicide so as to form a first final metal silicide and a second final metal silicide, respectively.

3. The method according to Claim 2, wherein the final annealing step is carried out at a temperature above about 650°C so as to form $CoSi_2$ as first final metal silicide and second final metal silicide.

4. The method according to Claim 1, wherein the first metal and the second metal are identical.

5. The method according to Claim 1, wherein the first metal and the second metal are different.

6. The method according to Claim 1, wherein the first metal and the second metal comprise at least one from the group formed by titanium, platinum, nickel, and cobalt.

7. The method according to Claim 1, wherein the hard mask is formed from at least one of titanium nitride and a silicon-germanium alloy.

8. The method according to Claim 1, wherein the formation of the first metal silicide comprises a deposition of the first metal on the drain and source regions, and a first initial annealing step.

9. The method according to Claim 7, wherein the first initial annealing step is carried out at a temperature below about 600°C so as to form CoSi as first metal silicide and second metal silicide.

10. The method according to Claim 1, wherein the formation of the second metal silicide comprises a deposition of the second metal on the gate region and on the first metal silicide, and a second initial annealing step.

11. The method according to Claim 10, wherein the second initial annealing step is carried out at a temperature below about 600°C so as to form CoSi as first metal silicide and second metal silicide.

12. The method according to Claim 1, wherein the source, drain and gate regions comprise silicon and in that the first metal and the second metal are cobalt.

13. The method according to Claim 12, wherein a first initial annealing step and a second initial annealing step are carried out at a temperature below about 600°C so as to form CoSi as first metal silicide and second metal silicide.

14. An integrated circuit that includes at least one transistor obtained by a method for fabricating a transistor with a metal gate, the method including a siliciding phase comprising:

the formation, from a first metal, of a first metal silicide on the drain and source regions, while the gate region is protected by a layer of hard mask;

the removal of the hard mask;

the formation, from a second metal, of a second metal silicide in the entire gate region so as to completely siliciding the gate region, while the first metal silicide is protected by the second metal; and

the removal of the second metal.

15. A process for producing a metal gate of a transistor, which process comprises the complete siliciding of the gate region.

16. The process according to claim 15, wherein complete siliciding of the gate region is decoupled from the siliciding of the source and drain regions.